UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,981	03/01/2004	Sanjay Bhardwaj	04303/000N238-US0	2112

20350 7590 06/23/2009

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
AHMED, ENAM	
ART UNIT	**PAPER NUMBER**
2112	

MAIL DATE	DELIVERY MODE
06/23/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/790,981	BHARDWAJ, SANJAY	
	Examiner	Art Unit	
	ENAM AHMED	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final

- This office action is in response to the applicant's amendment filed on 4/14/09
- The 35 U.S.C. 101 rejections are withdrawn due to cancellation of claims 1-3, 8-9 and 20.

Response to applicant's amendment

The applicants arguments have been fully considered, however are found persuasive only to the extent that new reference Grivna (U.S. Patent No. 6,539,051) teaches a first register for receiving a second output of the parallel framed data from the serial to parallel converter (column 8, lines 49-57); a second register for receiving a first output of the parallel framed data from the first register (column 8, lines 49-57); a first selector for selecting a portion of the first output of the parallel framed data and a portion of the second output of the parallel framed data to form a data word wherein the data word is a concatenation of the portion of the first and second outputs of the parallel framed data (column 10, lines 44-56); a second selector for selecting a first one of the second output of parallel framed data and the concatenated data word (see fig.5 and (column 10, line 44-column 11, line 12); a third selector for selecting a portion of the data held in the rotator and a portion of data held in the third register to form a data output comprising multiple frames of the serialized framed data (see fig.5 and (column 10, line 44-column 11, line 12) and a state machine, determining if the device is in a state of synchronization based on the counting mechanism, said state machine further causing the second selector to select a second one of the second output of parallel framed data and the concatenated data word

if the device is determined to not be in a state of synchronization (column 11, line 26 – column 12, line 10).

Response to applicant's remarks

On page 6, the applicant states claim 10 as amended is not taught by any of the references cited by the Examiner.

The Examiner respectfully only agrees to the extent that the above mentioned limitations as amended are not taught by the cited references. However, new reference Grivna (U.S. Patent No. 6,539,051) was applied against the amended limitations as seen above. As, from the previous action Taborek, Sr. et al. teaches a serial to parallel converter for converting the serialized framed data to a parallel framed data (column 3, lines 17-25); a guesser for guessing a position of a frame boundary in the data selected by the second selector (column 5, line 61 – column 6, line 6) and a tester for testing the data output to determine if the frame boundaries are at [[a]] predetermined positions in the data output (column 6, lines 6-21). Further, as from the previous action the Wright et al. reference teaches a rotator for rotating the selected data in accordance with the position guessed by the guesser (column 2, line 57 – column 3, line 10) and (column 3, lines 42-52) and a register for storing a delayed version f the rotated data (column 6, line 6 – column 7, line 6). Further, as from the previous action the Kaufman reference teaches a counting mechanism for counting when[[the]] a frame boundary is at[[the]] a predetermined position in the data output and further counting when a frame boundary is not at a predetermined position

(column 6, line 48 - column 7, line 4), (column 11, line 49 - column 12, line 2) and (column 12, lines 12-34).

35 U.S.C. 103 Rejections

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 13-16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049) in view of Kaufmann (U.S. Patent No. 5,483,539).

With respect to claim 10, the Taborek, Sr. et al. reference teaches a serial to parallel converter for converting the serialized framed data to a parallel framed data (column 3, lines 17-25); a guesser for guessing a position of a frame boundary in the data selected by the second selector (column 5, line 61 – column 6, line 6) and a tester for testing the data output to determine if the frame boundaries are at [[a]] predetermined positions in the data output (column 6, lines 6-21). The Taborek, Sr. et al. reference does not teach a first register for receiving a second output of the parallel framed data from the

serial to parallel converter; a second register for receiving a first output of the parallel framed data from the first register; a first selector for selecting a portion of the first output of the parallel framed data and a portion of the second output of the parallel framed data to form a data word wherein the data word is a concatenation of the portion of the first and second outputs of the parallel framed data; a second selector for selecting a first one of the second output of parallel framed data and the concatenated data word; a rotator for rotating the selected data in accordance with the position guessed by the guesser; a register for storing a delayed version f the rotated data; a third selector for selecting a portion of the data held in the rotator and a portion of data held in the third register to form a data output comprising multiple frames of the serialized framed data; a counting mechanism for counting when[[the]] a frame boundary is at[[the]] a predetermined position in the data output and further counting when a frame boundary is not at a predetermined position and a state machine, determining if the device is in a state of synchronization based on the counting mechanism, said state machine further causing the second selector to select a second one of the second output of parallel framed data and the concatenated data word if the device is determined to not be in a state of synchronization. The Grivna reference teaches a first register for receiving a second output of the parallel framed data from the serial to parallel converter (column 8, lines 49-57); a second register for receiving a first output of the parallel framed data from the first register (column 8, lines 49-57); a first selector for selecting a portion of the first output of the parallel framed data and a portion of the second output of the parallel framed data to form a data word wherein the data word is a concatenation of the portion of the first and

second outputs of the parallel framed data (column 10, lines 44-56); a second selector for selecting a first one of the second output of parallel framed data and the concatenated data word (see fig.5 and (column 10, line 44-column 11, line 12); a third selector for selecting a portion of the data held in the rotator and a portion of data held in the third register to form a data output comprising multiple frames of the serialized framed data (see fig.5 and (column 10, line 44-column 11, line 12) and a state machine, determining if the device is in a state of synchronization based on the counting mechanism, said state machine further causing the second selector to select a second one of the second output of parallel framed data and the concatenated data word if the device is determined to not be in a state of synchronization (column 11, line 26 – column 12, line 10). The Wright et al. reference teaches a rotator for rotating the selected data in accordance with the position guessed by the guesser (column 2, line 57 – column 3, line 10) and (column 3, lines 42-52) and a register for storing a delayed version f the rotated data (column 6, line 6 – column 7, line 6). The Kaufman reference teaches a counting mechanism for counting when[[the]] a frame boundary is at[[the]] a predetermined position in the data output and further counting when a frame boundary is not at a predetermined position (column 6, line 48 - column 7, line 4), (column 11, line 49 - column 12, line 2) and (column 12, lines 12-34). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the references Taborek et al. and Grivna to incorporate a first register for receiving a second output of the parallel framed data from the serial to parallel converter; a second register for receiving a first output of the parallel framed data from the first register; a first selector for selecting a portion of the first output

of the parallel framed data and a portion of the second output of the parallel framed data to form a data word wherein the data word is a concatenation of the portion of the first and second outputs of the parallel framed data; a second selector for selecting a first one of the second output of parallel framed data and the concatenated data word; a third selector for selecting a portion of the data held in the rotator and a portion of data held in the third register to form a data output comprising multiple frames of the serialized framed data and a state machine, determining if the device is in a state of synchronization based on the counting mechanism, said state machine further causing the second selector to select a second one of the second output of parallel framed data and the concatenated data word if the device is determined to not be in a state of synchronization into the claimed invention. The motivation for a first register for receiving a second output of the parallel framed data from the serial to parallel converter; a second register for receiving a first output of the parallel framed data from the first register; a first selector for selecting a portion of the first output of the parallel framed data and a portion of the second output of the parallel framed data to form a data word wherein the data word is a concatenation of the portion of the first and second outputs of the parallel framed data; a second selector for selecting a first one of the second output of parallel framed data and the concatenated data word; a third selector for selecting a portion of the data held in the rotator and a portion of data held in the third register to form a data output comprising multiple frames of the serialized framed data and a state machine, determining if the device is in a state of synchronization based on the counting mechanism, said state machine further causing the second selector to select a second one of the second output of parallel framed data and the

concatenated data word if the device is determined to not be in a state of synchronization is for improved error recovery. Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the references Taborek et al. and Wright et al. to incorporate a rotator for rotating the selected data in accordance with the position guessed by the guesser and a register for storing a delayed version f the rotated data into the claimed invention. The motivation for a rotator for rotating the selected data in accordance with the position guessed by the guesser and a register for storing a delayed version f the rotated data is for improved system performance. Thus, it would also have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the references Taborek et al. and Kaufman to incorporate a counting mechanism for counting when[[the]] a frame boundary is at[[the]] a predetermined position in the data output and further counting when a frame boundary is not at a predetermined position into the claimed invention. The motivation for a counting mechanism for counting when[[the]] a frame boundary is at[[the]] a predetermined position in the data output and further counting when a frame boundary is not at a predetermined position is for improved system performance.

With respect to claim 13, all of the limitations of claim 10 have been addressed above. The Taborek, Sr. et al. reference does not teach wherein the portion of the first output of the parallel framed data comprises bits of the first parallel framed data starting at an offset of an odd number of bits from the first arriving serial bits, and the portion of the second output of the parallel framed data comprises the first arriving odd number of

bits from the second parallel framed data. The Grivna reference teaches wherein the portion of the first output of the parallel framed data comprises bits of the first parallel framed data starting at an offset of an odd number of bits from the first arriving serial bits, and the portion of the second output of the parallel framed data comprises the first arriving odd number of bits from the second parallel framed data (column 10, lines 44-56). Thus, it would have been obvious to have combine the references Taborek, Sr. et al. and Grivna to incorporate wherein the portion of the first output of the parallel framed data comprises bits of the first parallel framed data starting at an offset of an odd number of bits from the first arriving serial bits, and the portion of the second output of the parallel framed data comprises the first arriving odd number of bits from the second parallel framed data into the claimed invention. The motivation for wherein the portion of the first output of the parallel framed data comprises bits of the first parallel framed data starting at an offset of an odd number of bits from the first arriving serial bits, and the portion of the second output of the parallel framed data comprises the first arriving odd number of bits from the second parallel framed data is for improved system performance.

With respect to claim 14, all of the limitations of claim 13 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the odd number of bits is one. The Wright et al. reference teaches wherein the odd number of bits is one (column 2, lines 46-56). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to have combined the references Taborek, Sr. et al. reference and Wright et al. to incorporate wherein the odd number of bits is one into the

claimed invention. The motivation for wherein the odd number of bits is one is so cell delineation can be achieved. (Column 3, lines 50-51 – Wright et al. reference).

With respect to claim 15, the Taborek, Sr. et al. reference teaches wherein the serialized framed data comprises a plurality of frames, each frame comprising a data field and a synchronization pattern (column 8, lines 46-55).

With respect to claim 16, the Taborek, Sr. et al. reference teaches wherein the data field comprises 64b/66b (column 9, lines 10-27). The Taborek, Sr. et al. and Wright et al. references also addresses various aspects of ethernet technology that address field, synchronization, transmission and other aspects that make data field segmentation obvious to one skilled in the art.

With respect to claim 17, the Taborek, Sr. et al. reference teaches wherein the serialized data is a 10 Gb Ethernet data (column 2, line 55 – column 3, line 16).

Claims 11-12 are rejected under Taborek, Sr. et al. (U.S. 7,0202,729), Grivna (U.S. Patent No. 6,539,051), Wright et al. (U.S. Patent No. 7,103,049), Kaufmann (U.S. Patent No. 5,483,539) in view of Swoboda et al. (U.S. Patent No. 6,085,336).

With respect to claim 11, all of the limitations of claim 10 have been addressed. The Taborek, Sr. et al. reference does not teach an exhaust register, the exhaust register

storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser. The Swoboda et al. reference teaches an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser (column 38, lines 32-41). Thus it would have been obvious to have combined the references Taborek, Sr. et al. and Swoboda et al. references to incorporate an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser into the claimed invention. The motivation for an exhaust register, the exhaust register storing one or more positions guessed by the guesser determined not to contain a frame boundary at a position guessed by the guesser is to provide improved emulation, simulation and testability architectures and methods that are viable alternative to high capital-cost test equipment and systems (column 3, lines 25-27 – Swoboda et al. reference).

With respect to claim 12, all of the limitations of claim 11 have been addressed. The Taborek, Sr. et al. reference does not teach wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary. The Swoboda et al. reference teaches wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary (column 38, lines 58-65). Thus it would have been obvious to have combined the references Taborek, Sr. et al. and Swoboda et al. references to incorporate wherein the guesser excludes the one or more positions stored in the exhaust register as possible

positions of the frame boundary into the claimed invention. The motivation for wherein the guesser excludes the one or more positions stored in the exhaust register as possible positions of the frame boundary is to provide improved emulation, simulation and testability architectures and methods that are viable alternative to high capital-cost test equipment and systems (column 3, lines 25-27 – Swoboda et al. reference).

Conclusion

a. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman, can be reached on 571-272-3644.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

6/19/09

/MUJTABA K CHAUDRY/

Primary Examiner, Art Unit 2112